appended thereto is transferred to the CPU **1** and parity check circuit **10**. When the CPU **1** makes access to the I/O unit **3** for reading incoming data, the incoming signal **34** is read in through the photocoupler **31***a* and buffer **32**, and it is held in the latch **33***a* in accordance with the signal on the address command bus **7**. The parity generator **30** receives data from the latch **33***a* on the data bus **8**, generates a parity bit of even or odd parity mode, and appends the parity signal **14** to the data. Then the incoming data with the parity signal appended thereto is transferred to the CPU **1** and parity check circuit **10**.

Accordingly, when the CPU **1** reads data from the main storage **2** or I/O unit **3**, the parity signal **14** is transferred along with data to the parity check circuit **10** which performs a parity check of the data bits read out from the main storage or I/O unit with the parity signal **14**. If a parity error is detected as a result of the parity check, a parity error signal **11** is delivered as an interrupt request signal to the interrupt controller **12**, which in turn issues an interrupt request to the CPU **1**. The CPU **1** causes the program to branch to a preprogrammed interrupt routine, which sets the data being stored in the tracing memory memory for indicating a parity error along with the predetermined conventional trace information including the data bits on bus **8** and the logical state of a fault detection signal.

The trace function is designed to store tracing data in predetermined addresses in the tracing memory **41** without affecting the operation of the control system when the CPU **1** makes access to the main storage and I/O unit for the control operation. By means of the parity check circuit and the interrupt procedure, the parity error signal is also stored in the tracing memory.

The following describes the retrieval of tracing data stored in the tracing memory **41**. The CPU **1** executes a preprogrammed trace retrieval program to retrieve data in the tracing memory **41** corresponding to data from a predetermined address. The source address of data associated with a fault detected by conventional means is set in advance on the address setting switch **51** in the tracing memory retrieval unit **5**. The address comparator **52** operates to detect the coincidence of the address on the address bus **7** for the trace data provided by the CPU **1** with the address set on the address setting switch **51**, and data on the data bus **8** is latched when the coincidence is detected. The latched data is transferred as multi-bit signals **55** or converted into an analog signal by the D/A converter **54** and transferred to the instrumentation unit **6**, which then records the tracing data.

FIGS. **3** and **4** show data charts recorded by the instrumentation unit **6**. Each chart includes the record of a signal under trace **S10**, a fault detection signal **S11** and a parity error signal **S12**. In the case of FIG. **3**, the parity error is detected after the fault has been detected, while in the case of FIG. **4**, the fault is detected after the parity error has been detected.

Namely, in the case of FIG. **3**, it can be said that the fault detection signal itself has not been detected erroneously and the traced signal itself is reliable. Whereas, in the case of FIG. **4**, it can be considered that the fault detection signal has been detected erroneously and the traced signal at the time of parity error detection could differ from the actual signal.

These diagnoses, which have not been possible in the conventional fault tracing system, are made possible by the foregoing embodiment through the provision for storing the parity error signal in the tracing memory **4**. Accordingly, the present invention can effectively enhance the reliability of fault analysis through the inclusion of the parity error signal in signals under trace.

What is claimed is:

1. A fault determining apparatus for a data transmission system having a central processing unit (CPU) which transfers data to and from a main storage and an input/output unit through a data bus in accordance with information on an address command bus, said apparatus comprising:

parity generating means in each of said main storage and said input/output unit for generating and appending a parity bit to the data bus upon transfer of data bits from the respective main storage and input/output unit to the data bus,

parity checking means associated with the CPU and connected to the data bus for receiving the data bits and the parity bit and for generating a parity error signal when the parity of the received data bits does not correspond to the received parity bit,

a trace memory means connected to the data bus and the address command bus and including addressing means responsive to detection of predetermined signals on the address command bus for storing trace information of data received by said CPU from said main storage and said input/output units over a predetermined duration and for storing a transitional record of the logical state of a fault detection signal and the parity error signal from the parity checking means along with the stored data;

trace memory retrieval means for retrieving information stored in said trace memory means corresponding to stored data from a selected source address of said main storage and said input/output means along with the corresponding stored transitional record of the fault detection signal and the parity error signal; and

means for generating a record of said data transmission system based on said retrieved data and transitional record of said fault detection signal and said parity error signal retrieved by said trace memory retrieval means.

2. An apparatus according to claim **1**, wherein said main storage comprises a random access memory (RAM) and a read-only memory (ROM) connected to the data bus and the address command bus along with the parity generating means for the main storage for generating and transferring the data bits and the parity bit to the data bus when the address command bus calls for transfer of data from an address in said RAM or ROM.

3. An apparatus according to claim **1**, wherein said input/output unit comprises an input photocoupler, a buffer register connected to the output of the photocoupler, and a latch register connected to the buffer register and the address command bus for applied input data bits to the data bus and the parity generating means of the input/output means.

4. An apparatus according to claim **1**, wherein said trace memory means comprises a trace memory connected to the data bus, an address converting circuit connected to the address command bus for detecting predetermined address signals to generate lesser significant address bits for the trace memory in correspondence to accessing by the CPU of selected addresses of interest called for at steps within a cyclic operating procedure, a counter stepped at completion of each cyclic operating procedure to generate greater signifi-